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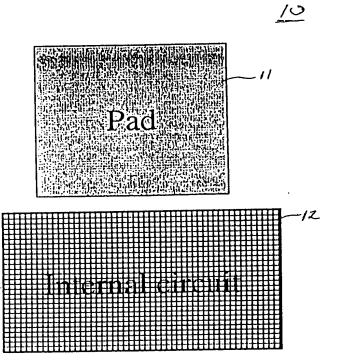
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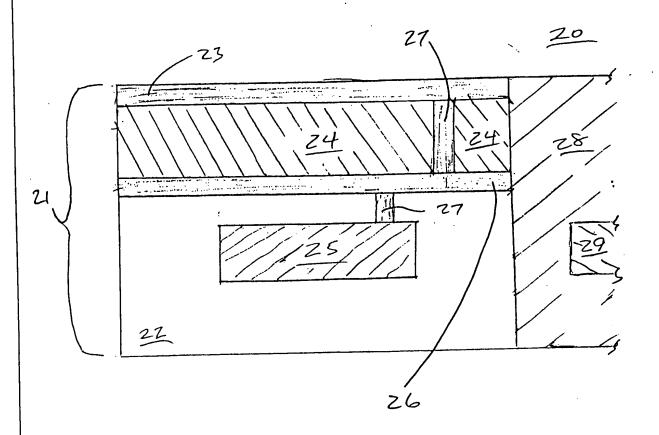
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SCREDTLER® Engineer's Computation Pad



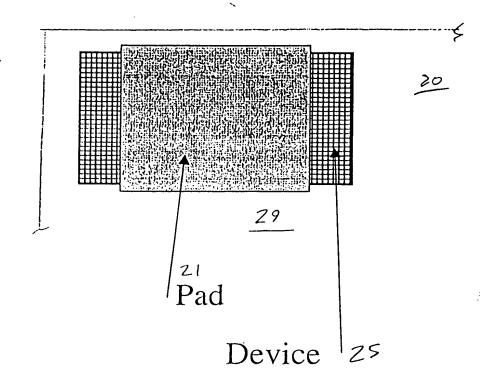
Top side view

(CONVENTIONAL ART)
Fig. 1



Fis. 2

SCAEDTLER* No. 937 811E Engineer's Computation Pad

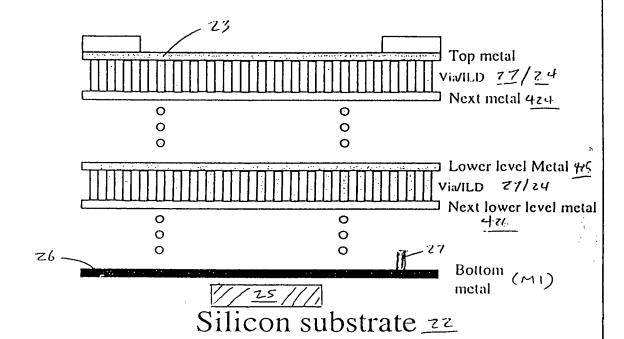


Top side view

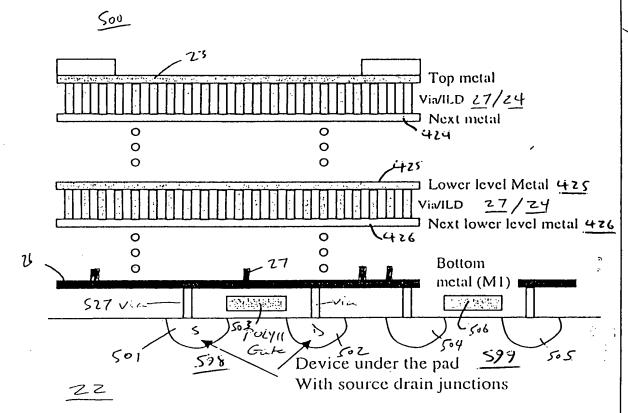
Of internal circuit

Fig. 3

4.00



Cross section view



Cross section view

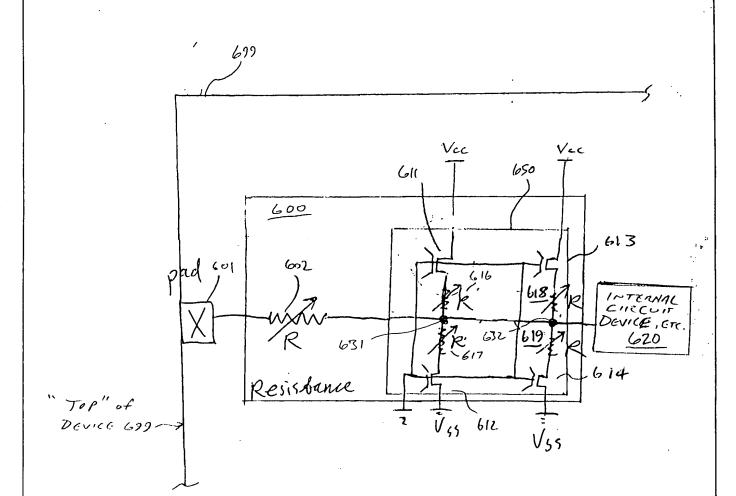


Fig. 6

700 14L 743. The number of these vias are adjusted To achieve the best resistance for the Drain junction Top metal WiWILD 724 Next metal 731 0 0 E Lower level Metal 732 4WILD 724 Next lower level metal 733 0 0 0 Bottom mctal (M1) 706 31 1 15 11 712 711 Device under the pad With source drain junctions 722

Cross section view

Gia, 7

80 Fabricating a Semiconductor Structure with ESD Protection

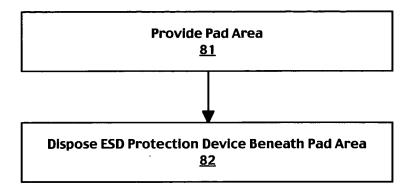


Fig. 8

90 Fabricating a Semiconductor Structure

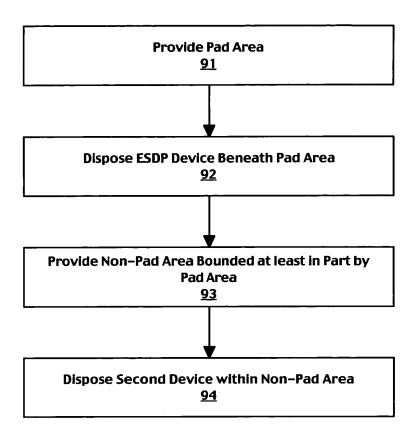


Fig. 9

100 Fabricating a Pad Area

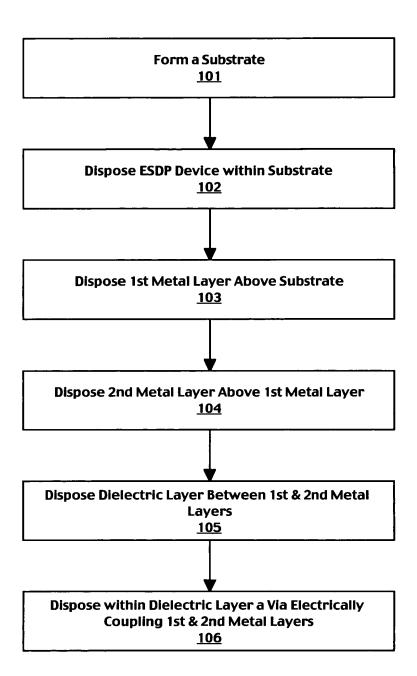


Fig. 10

1100 Fabricating a Pad Area with ESD Protective Device Below

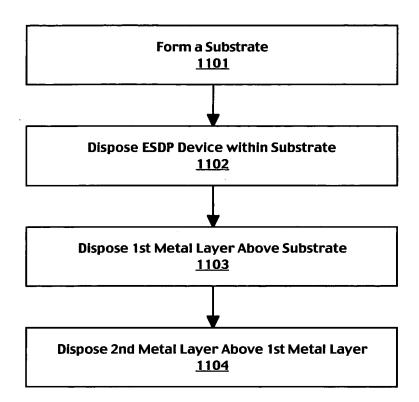


Fig. 11

1200 Fabricating a Pad Area with ESDP Below

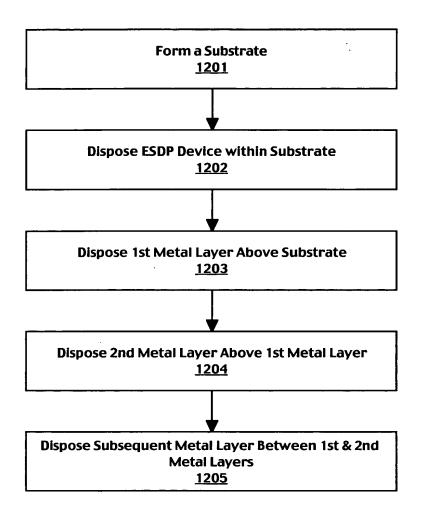


Fig. 12

1300 Fabricating an ESDP Device

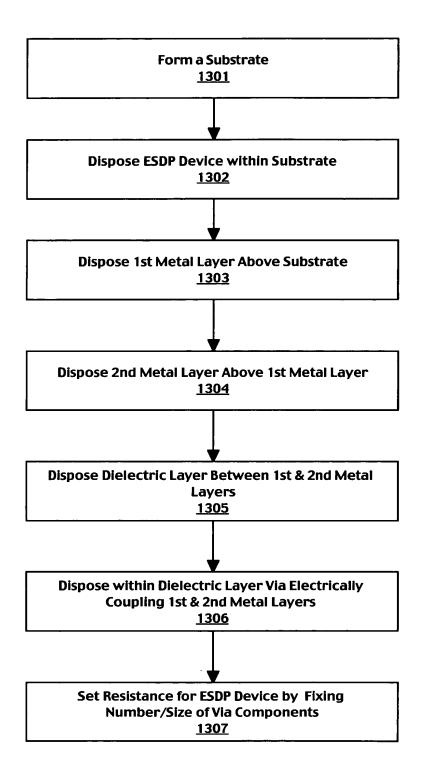


Fig. 13